Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/31/11 has been entered.

2. The amendment filed 1/31/11 has been considered and entered. Claims 1-22 have been canceled. Claims 27-31 have been added. Claims 26-31 remain in the application.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 28,30 and 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims 28,30 and 31 are duplicate of claims 23,25 and 26 and therefore are not further limiting. Both claims require the first and second liquid patterns that make up a single layer be applied in a single plane. Clarification is requested.

Claim Rejections - 35 USC § 103

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 23-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furusawa et al. (7,285,305) (a) alone or (b) in combination with Lee et al. (2004/0045657) both (a) or (b) further in combination with JP 11-163499 or JP 11-274671.

Furusawa et al. (7,285,305) teaches a multilayered wiring board and method of producing the multilayered wiring board. Furusawa et al. (7,285,305) teaches polyamide insulating layers (22) between the wiring layers and an interlayer conducting post (18) for conducting between wiring pattern (17) and the wiring pattern (31) wherein the insulating layer is disposed around the conducting post (18) using a liquid drop discharge system (abstract). Looking at the Figs, conductive wirings (17) are formed with conductive posts (18) and then insulating layer is formed surround the posts (18). Then wiring layers (31) and posts (32) are formed that connect to the wiring layer (17) and insulating layer (33) is applied to surround the post (32).

Furusawa et al. (7,285,305) fails to teach first forming the insulating portion of the first layer and then the conductive layer but teaches the reverse of this process.

(a)While the Examiner acknowledges the fact that the claimed invention teaches process steps of forming the conductor and then insulator patterns as opposed to forming the insulator and then conductive patterns, it is the Examiner's position that one skilled in the art at the time the invention was made would have had a reasonable expectation of achieving similar success regardless of which layer was applied first and which layer was applied subsequently as long as both conductive and insulative layers are formed within the same layer as claimed.

(b) Lee et al. (2004/0045657) teaches method of forming a multilayer ceramic electronic device whereby a dielectric sheet with a pattern of via holes is formed on a conductive layer and

subsequently the pattern of vias holes are filled with conductive paste (Figs. 1B-1D and Fig. 2). The dielectric and conductive layers are formed by printing ([0004]).

Therefore it would have been obvious for one skilled I the art at the time the invention was made to have modified Furusawa et al. (7,285,305) process by first forming the dielectric layer and then filling with conductor paste as opposed to forming conductor layer first and then dielectric layer surrounding the conductor as evidenced by Lee et al. (2004/0045657) with the expectation of achieving similar success, i.e. a layer including conductive and dielectric portions.

Furusawa et al. (7,285,305) (a) alone or (b) in combination with Lee et al. (2004/0045657) fail to teach the first and or second layer including conductive and insulating material being in a single plane.

JP 11-163499 teaches manufacturing a conductor pattern whereby conductive pattern and insulative material are formed by ink-jet printing in a single plane (abstract and Figs. 1b,2b and 3b)

JP 11-274671 teaches electric circuit and manufacturing thereof whereby conductor and insulator material are formed on a substrate in a single plane (abstract and Figs. 20-22).

Therefore it would have been obvious for one skilled in the art at the tem the invention was made to have modified Furusawa et al. (7,285,305) (a) alone or (b) in combination with Lee et al. (2004/0045657) process to form the conductor/insulative patterned layers in a single plane as evidenced by JP 11-163499 or JP 11-274671 with the expectation of achieving similar success.

Response to Amendment

8. Applicant's arguments with respect to claims 23-31 have been considered but are moot in view of the newly applied rejection.

Applicant argued Furusawa et al. (7,285,305) (a) alone or (b) in combination with Lee et al. (2004/0045657) fail to teach the first and or second layer including conductive and insulating material being in a single plane.

JP 11-163499 and JP 11-274671 teach this limitation as detailed above.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian K. Talbot whose telephone number is (571) 272-1428. The examiner can normally be reached on Monday-Friday 8AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy H. Meeks can be reached on (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brian K Talbot/
Primary Examiner, Art Unit 1715

BKT